Fig. 1A

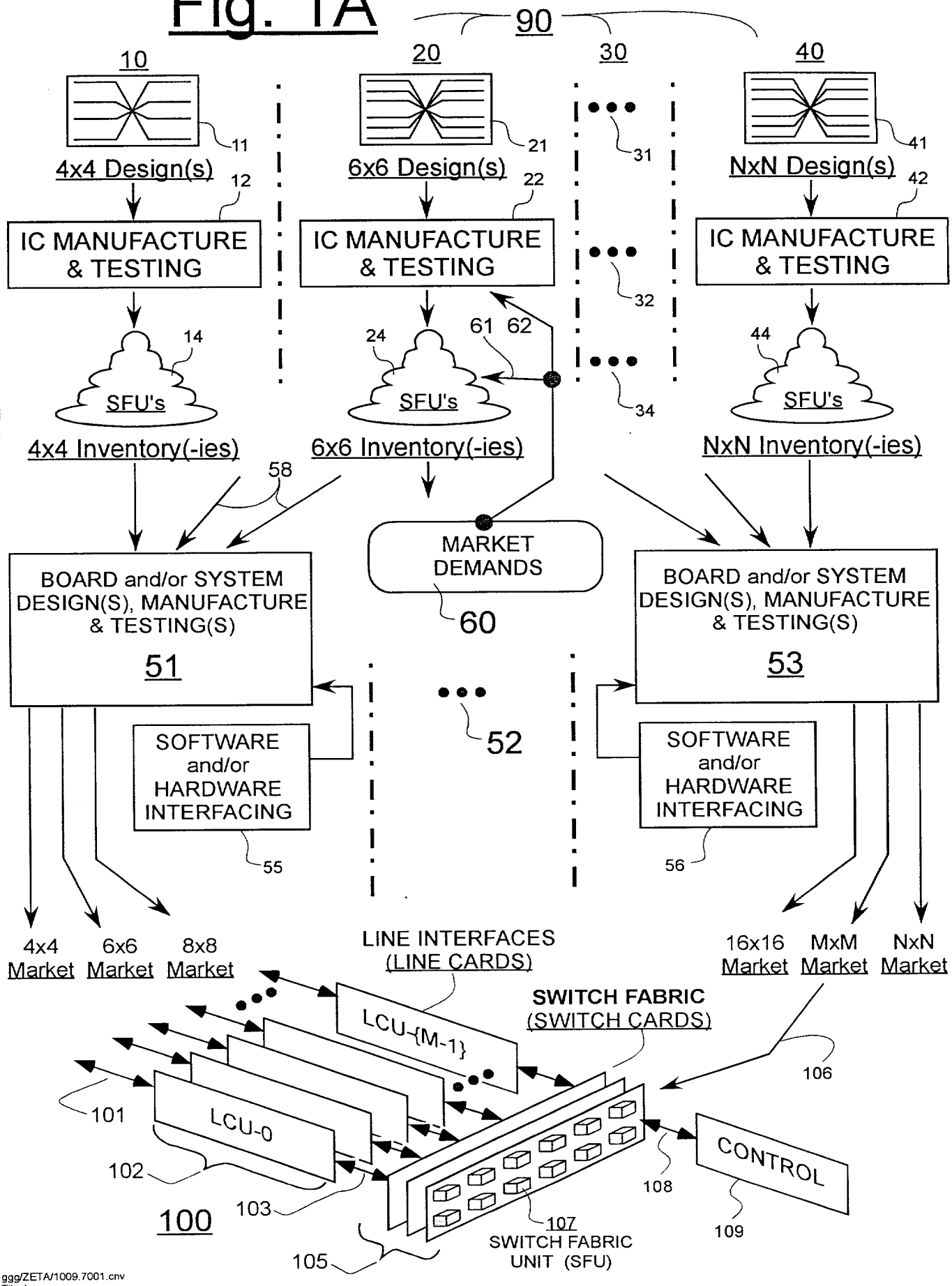

90
10
20
30
40
11
21
31
41
4x4 Design(s)
6x6 Design(s)
NxN Design(s)
12
22
42
IC MANUFACTURE & TESTING
IC MANUFACTURE & TESTING
IC MANUFACTURE & TESTING
32
14
24
61
62
44
SFU's
SFU's
SFU's
34
4x4 Inventory(-ies)
6x6 Inventory(-ies)
NxN Inventory(-ies)
58
MARKET DEMANDS
60
BOARD and/or SYSTEM DESIGN(S), MANUFACTURE & TESTING(S)
51
BOARD and/or SYSTEM DESIGN(S), MANUFACTURE & TESTING(S)
53
52
SOFTWARE and/or HARDWARE INTERFACING
55
SOFTWARE and/or HARDWARE INTERFACING
56
4x4 Market
6x6 Market
8x8 Market
LINE INTERFACES (LINE CARDS)
16x16 Market
MxM Market
NxN Market
SWITCH FABRIC (SWITCH CARDS)
106
LCU-{M-1}
101
LCU-0
102
CONTROL
108
100
103
107
SWITCH FABRIC UNIT (SFU)
109
105

Fig. 1B

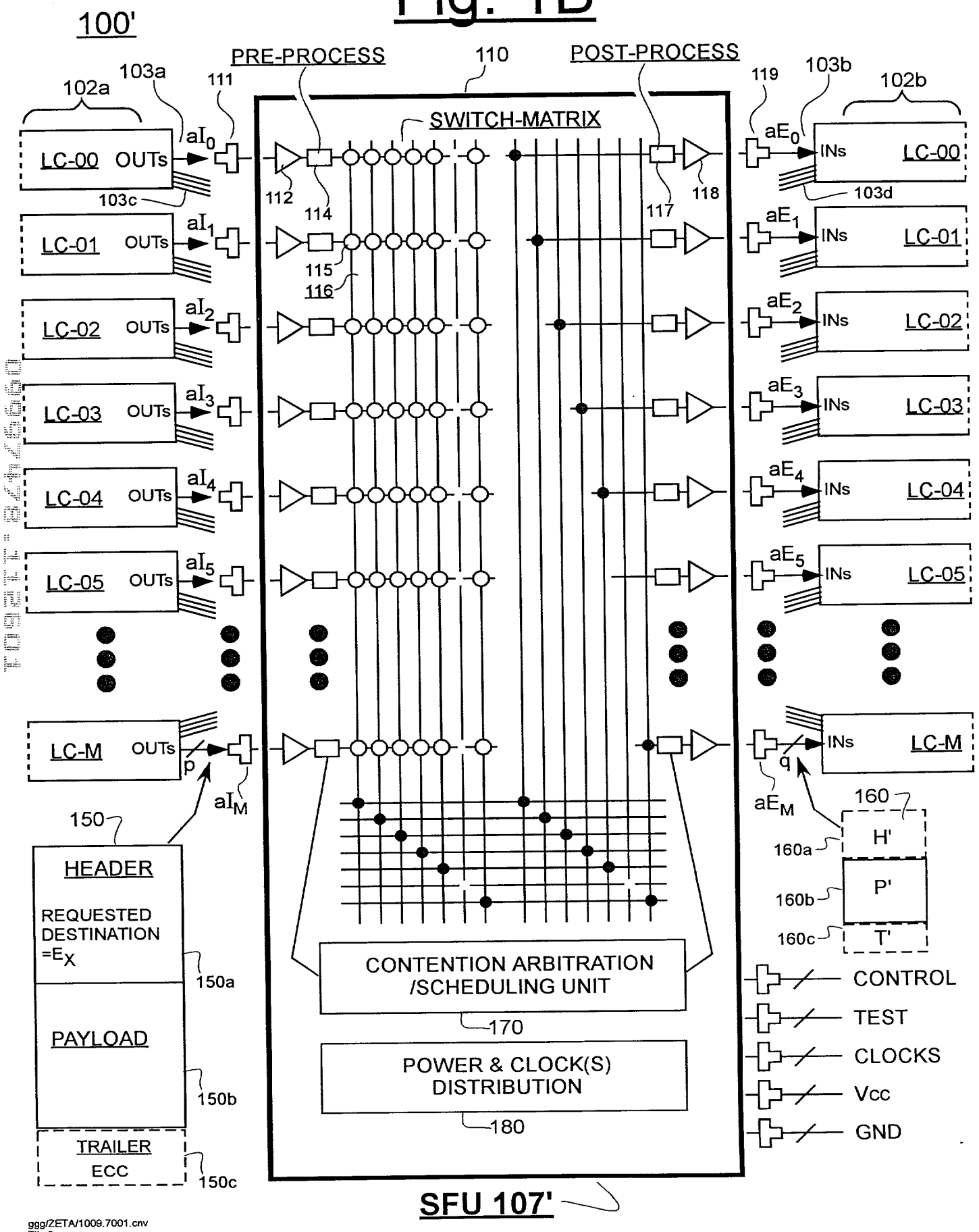

100'
PRE-PROCESS
110
POST-PROCESS
SWITCH-MATRIX
102a
103a
111
119
103b
102b
LC-00 OUTs
aI0
aE0
INs LC-00
103c
103d
112
114
117
118
LC-01 OUTs
aI1
aE1
INs LC-01
115
116
LC-02 OUTs
aI2
aE2
INs LC-02
LC-03 OUTs
aI3
aE3
INs LC-03
LC-04 OUTs
aI4
aE4
INs LC-04
LC-05 OUTs
aI5
aE5
INs LC-05
LC-M OUTs
p
aIM
INs LC-M
q
aEM
150
160
HEADER
REQUESTED DESTINATION =EX
150a
160a
H'
160b
P'
160c
T'
PAYLOAD
150b
TRAILER
ECC
150c
CONTENTION ARBITRATION /SCHEDULING UNIT
170
POWER & CLOCK(S) DISTRIBUTION
180
CONTROL
TEST
CLOCKS
Vcc
GND
SFU 107'

Fig. 2A

200

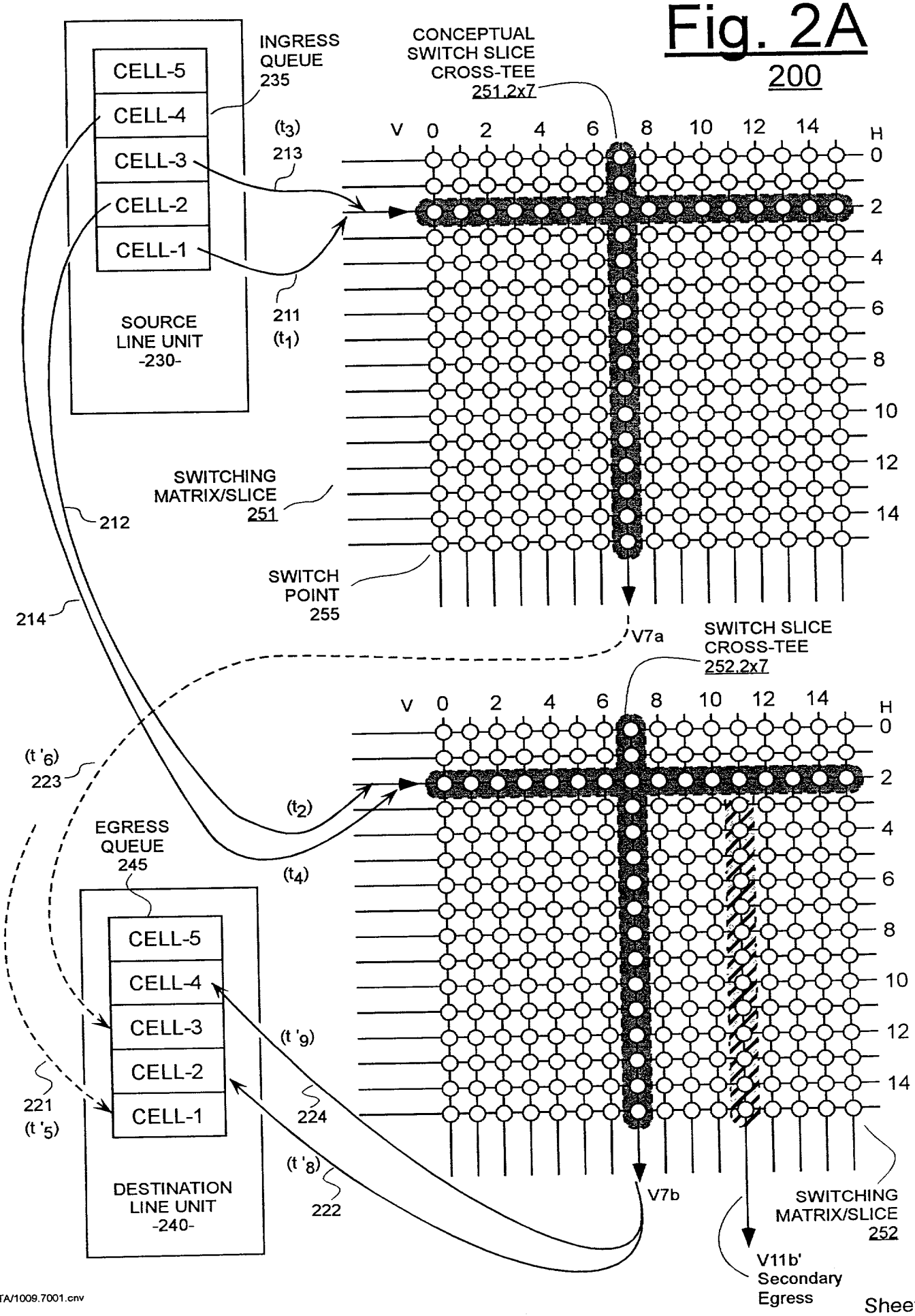


Fig. 2B

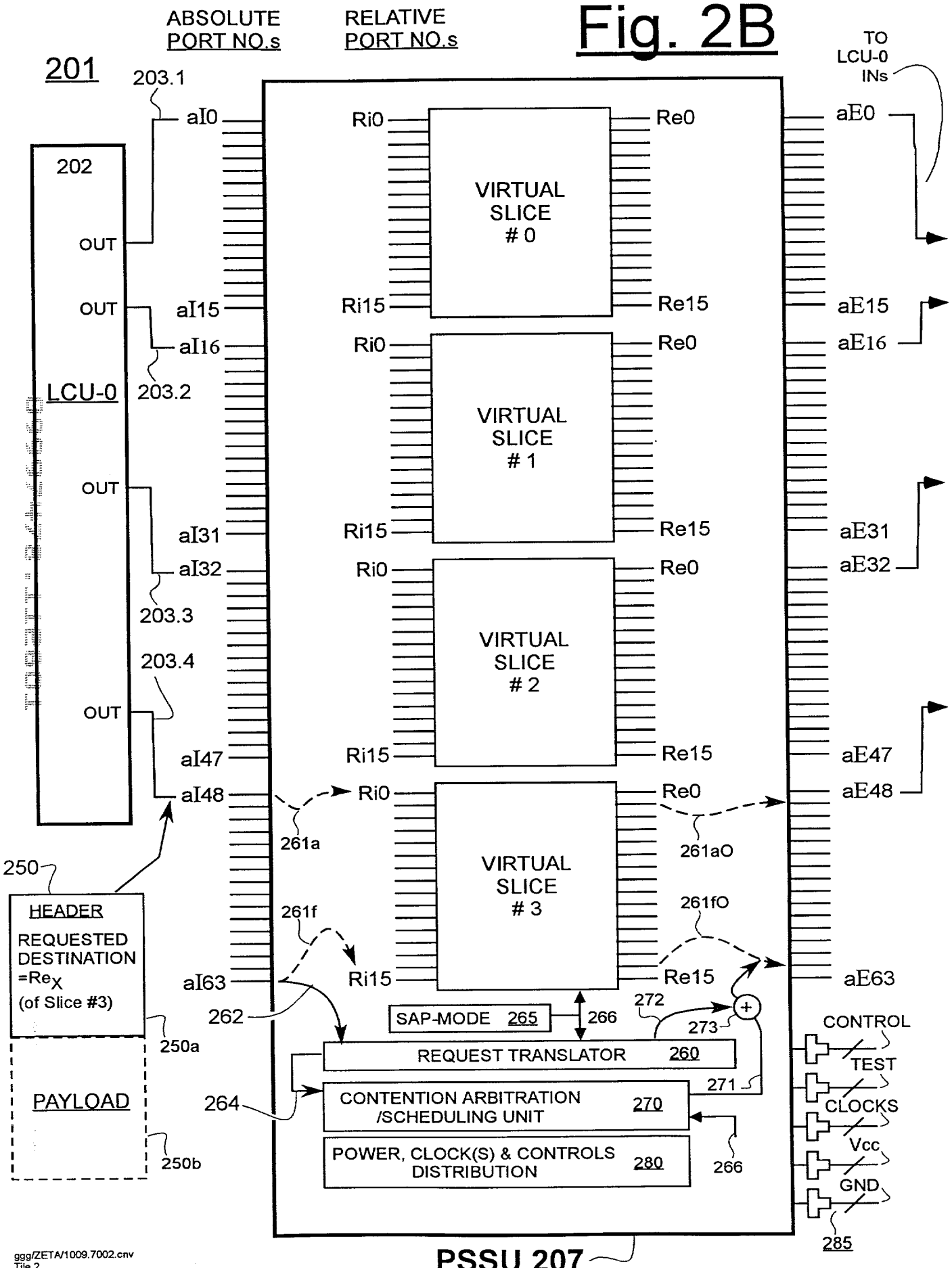
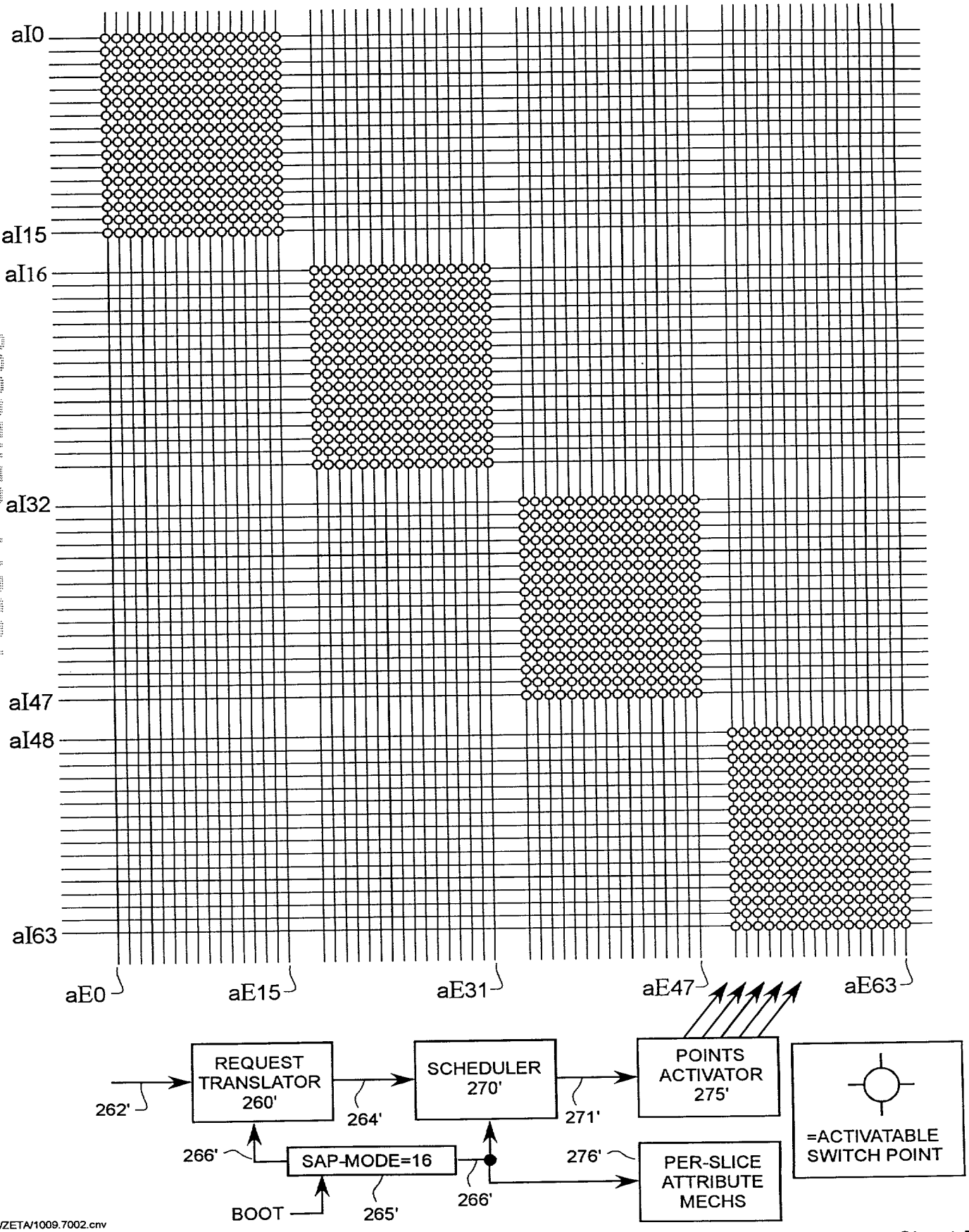

ABSOLUTE PORT NO.s
RELATIVE PORT NO.s
201
203.1
aI0
202
OUT
OUT
aI15
aI16
LCU-0
203.2
OUT
aI31
aI32
203.3
203.4
OUT
aI47
aI48
250
HEADER
REQUESTED DESTINATION =ReX (of Slice #3)
250a
PAYLOAD
250b
261a
261f
aI63
262
Ri0
Re0
Ri15
Re15
VIRTUAL SLICE # 0
VIRTUAL SLICE # 1
VIRTUAL SLICE # 2
VIRTUAL SLICE # 3
261aO
261fO
SAP-MODE 265
266
272
273
REQUEST TRANSLATOR 260
271
264
CONTENTION ARBITRATION /SCHEDULING UNIT 270
POWER, CLOCK(S) & CONTROLS DISTRIBUTION 280
266
TO LCU-0 INs
aE0
aE15
aE16
aE31
aE32
aE47
aE48
aE63
CONTROL
TEST
CLOCKS
Vcc
GND
285
PSSU 207

Fig. 2C

207'

SAP-16 MODE (25% SLICES)



207"

Fig. 2D

SAP-32 MODE (50% SLICES)

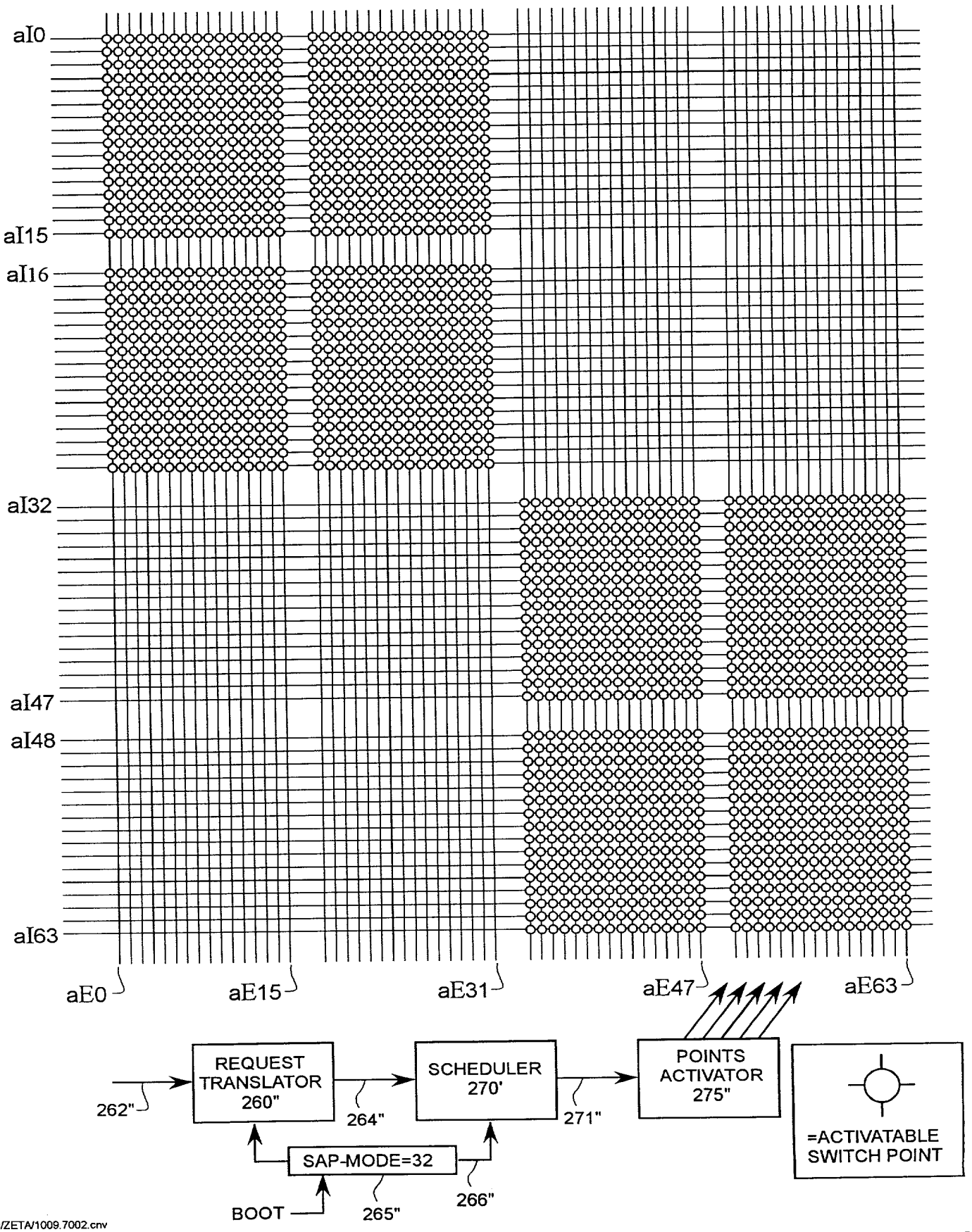


Fig. 2E

207'''

MIXED SLICES

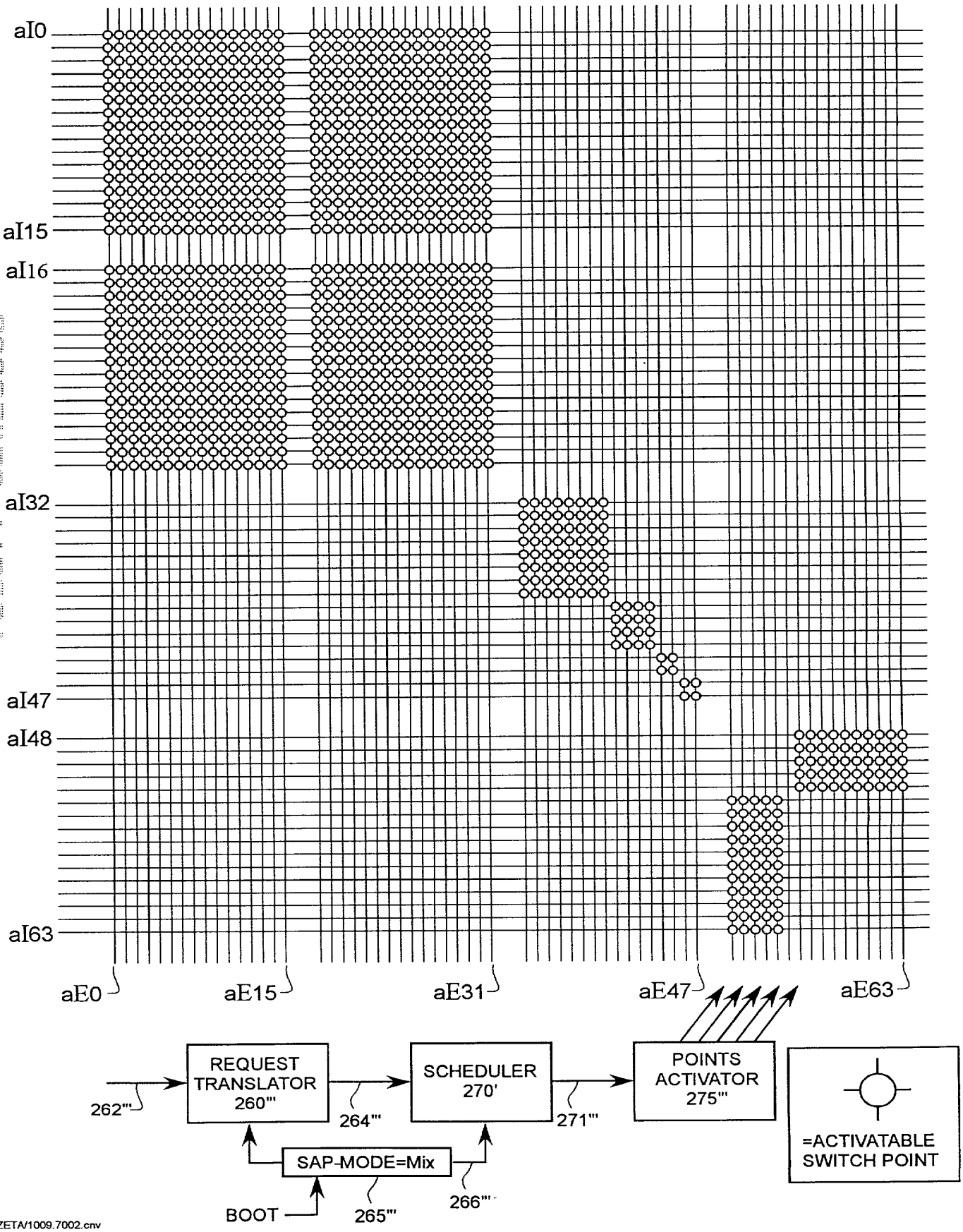


Fig. 3A

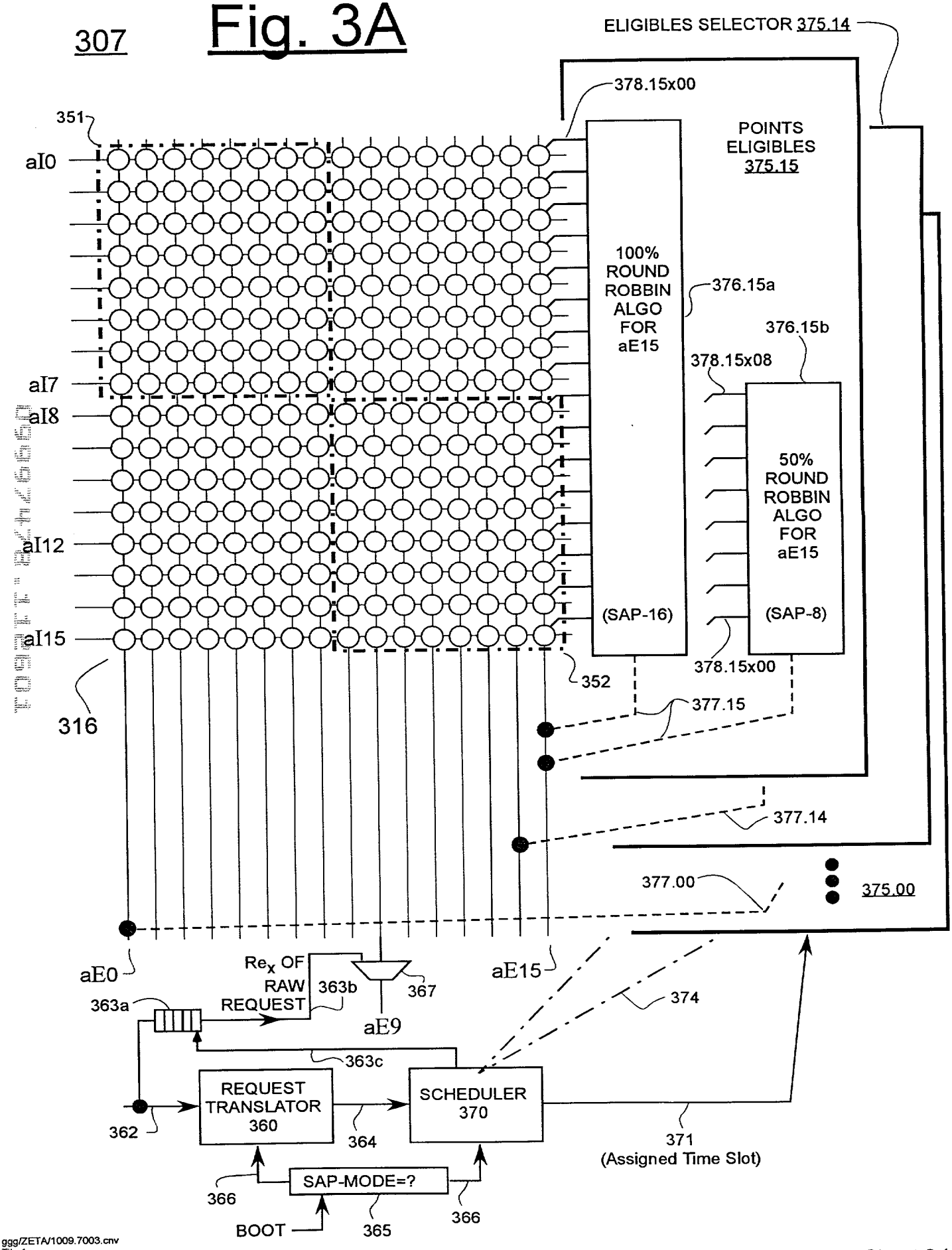

307
ELIGIBLES SELECTOR 375.14
378.15x00
351
aI0
aI7
aI8
aI12
aI15
316
352
POINTS ELIGIBLES 375.15
100% ROUND ROBBIN ALGO FOR aE15
376.15a
376.15b
378.15x08
50% ROUND ROBBIN ALGO FOR aE15
(SAP-16)
(SAP-8)
378.15x00
377.15
377.14
377.00
375.00
aE0
aE15
Rex OF RAW REQUEST
363a
363b
367
aE9
374
363c
REQUEST TRANSLATOR 360
SCHEDULER 370
362
364
371
(Assigned Time Slot)
SAP-MODE=?
366
366
BOOT
365

Fig. 3B

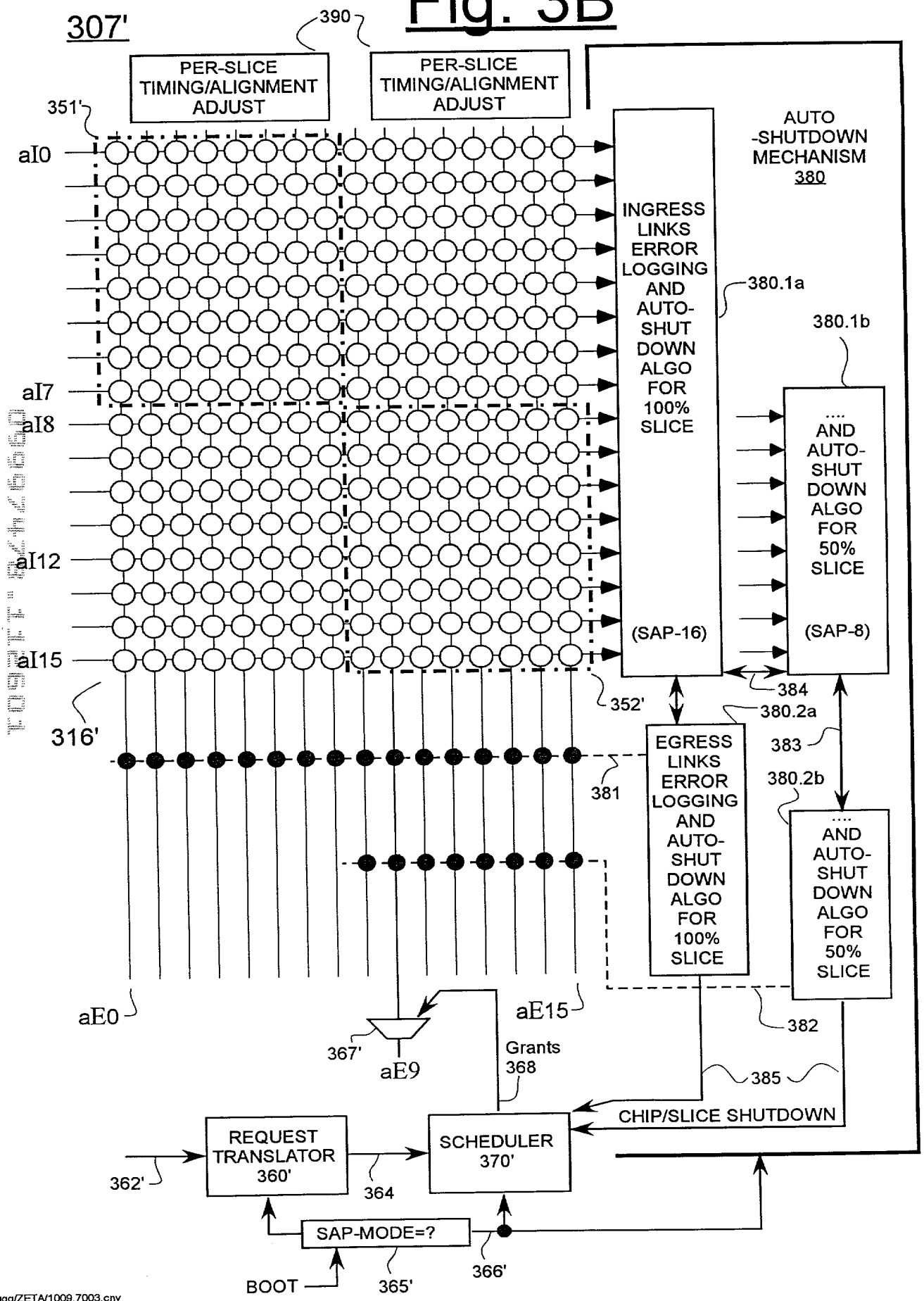
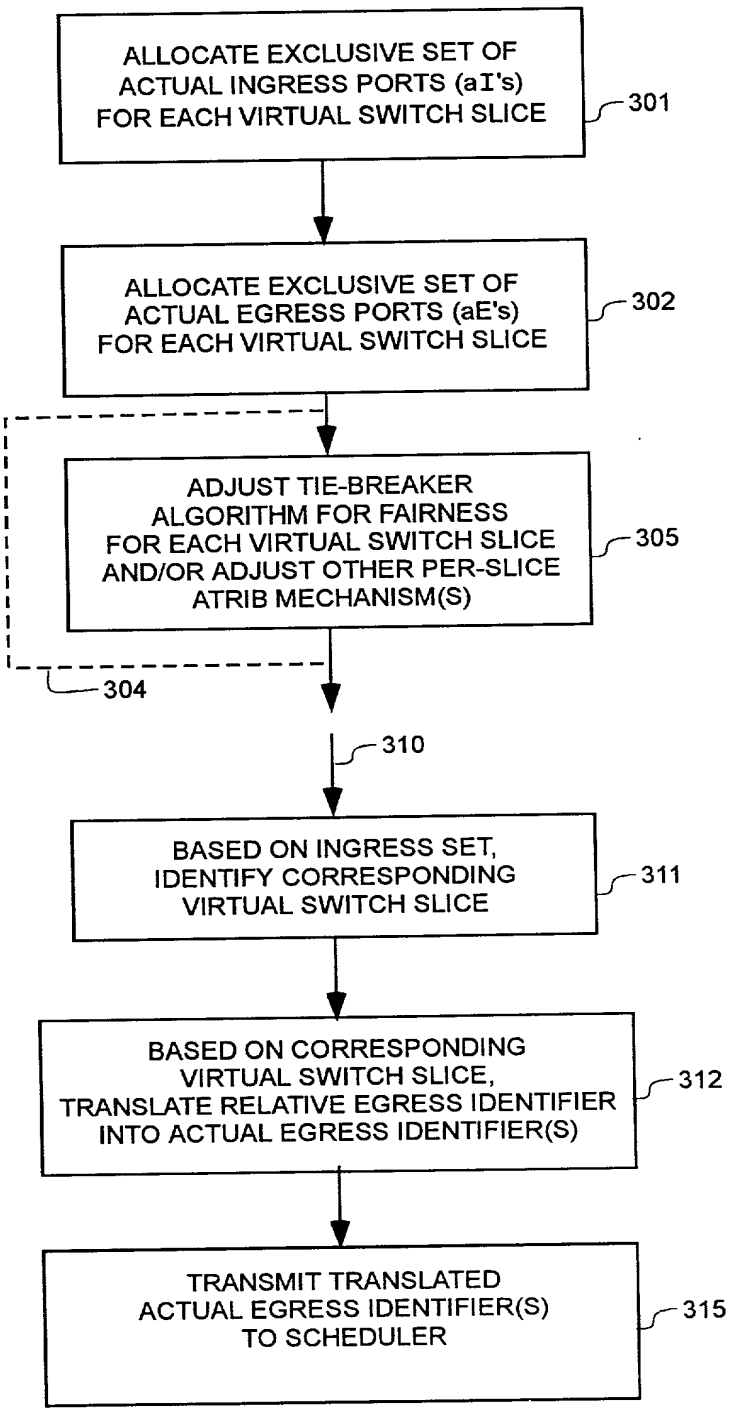

307'
390
PER-SLICE TIMING/ALIGNMENT ADJUST
PER-SLICE TIMING/ALIGNMENT ADJUST
351'
aI0
aI7
aI8
aI12
aI15
316'
INGRESS LINKS ERROR LOGGING AND AUTO-SHUT DOWN ALGO FOR 100% SLICE
(SAP-16)
AUTO -SHUTDOWN MECHANISM 380
380.1a
380.1b
.... AND AUTO-SHUT DOWN ALGO FOR 50% SLICE
(SAP-8)
352'
384
380.2a
383
380.2b
EGRESS LINKS ERROR LOGGING AND AUTO-SHUT DOWN ALGO FOR 100% SLICE
.... AND AUTO-SHUT DOWN ALGO FOR 50% SLICE
381
382
aE0
aE15
367'
aE9
Grants 368
385
CHIP/SLICE SHUTDOWN
REQUEST TRANSLATOR 360'
362'
364
SCHEDULER 370'
SAP-MODE=?
BOOT
365'
366'

Fig. 3C

300



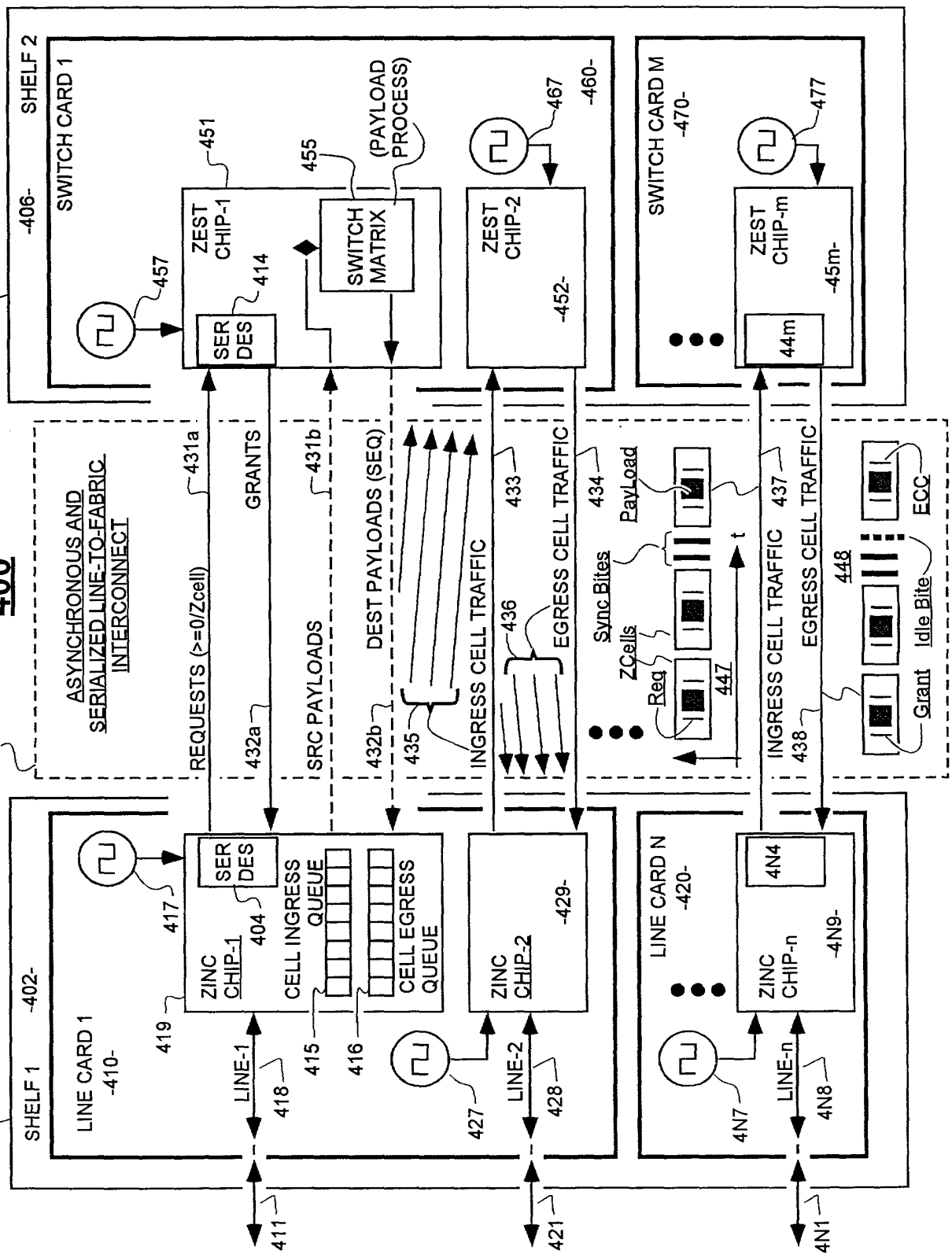
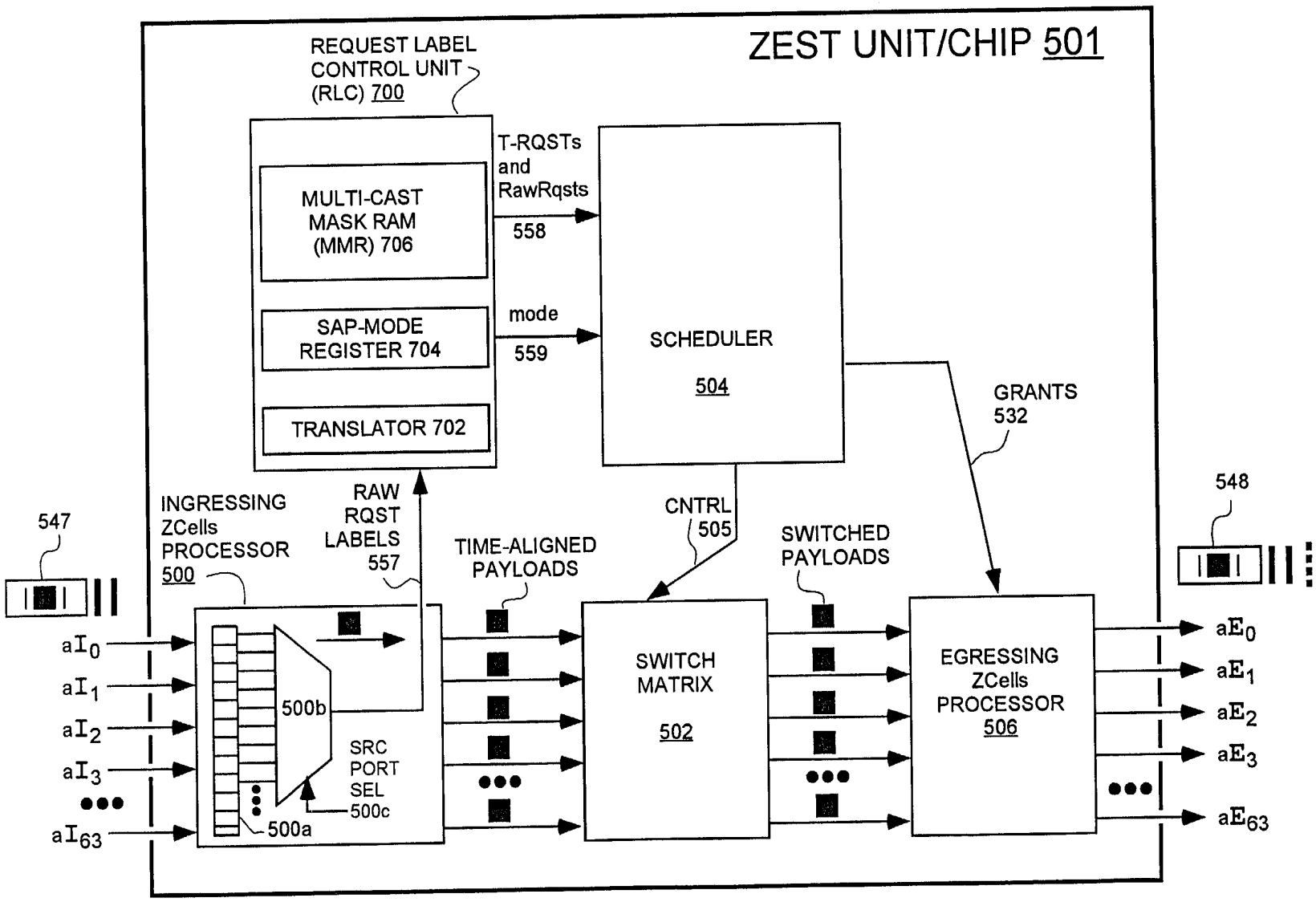
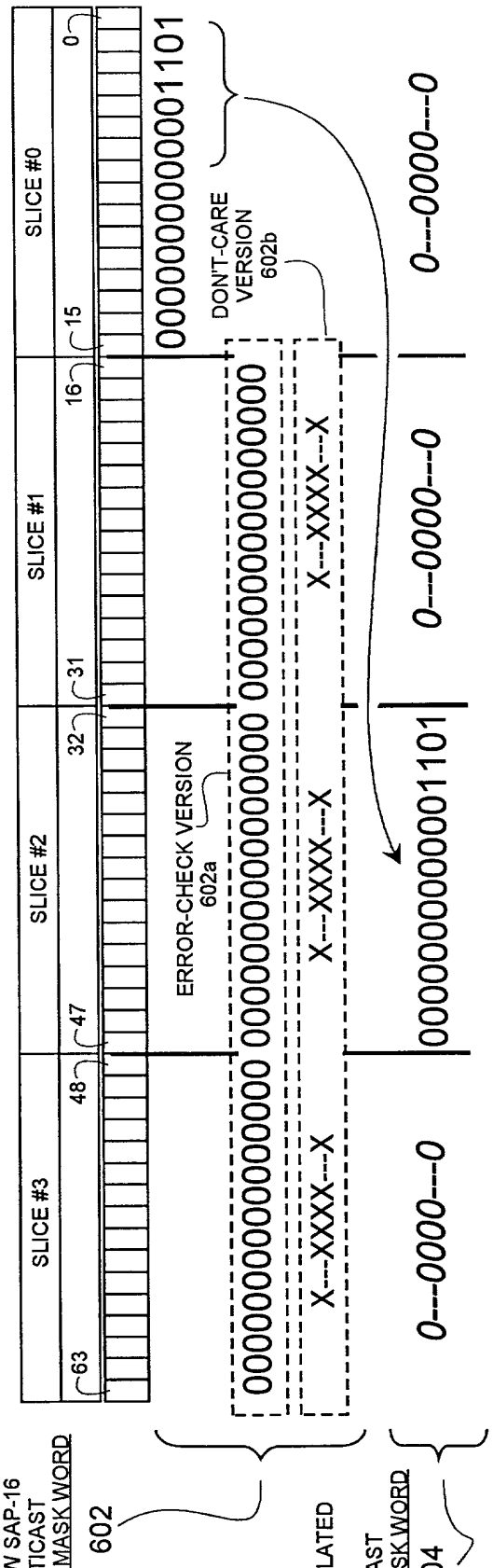


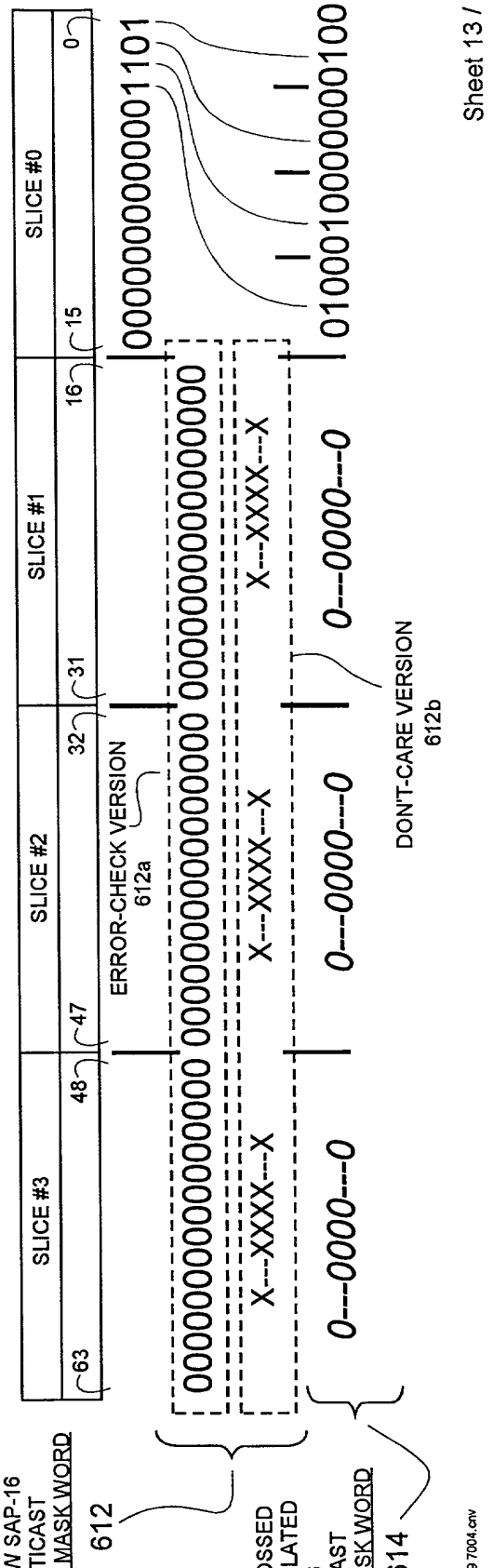
Fig. 4

Sheet 11 /

Fig. 5


ZEST UNIT/CHIP 501
REQUEST LABEL CONTROL UNIT (RLC) 700
MULTI-CAST MASK RAM (MMR) 706
SAP-MODE REGISTER 704
TRANSLATOR 702
T-RQSTs and RawRqsts
558
mode
559
SCHEDULER
504
GRANTS
532
547
548
INGRESSING ZCells PROCESSOR 500
RAW RQST LABELS 557
TIME-ALIGNED PAYLOADS
CNTRL 505
SWITCHED PAYLOADS
aI0
aI1
aI2
aI3
aI63
500b
SRC PORT SEL 500c
500a
SWITCH MATRIX 502
EGRESSING ZCells PROCESSOR 506
aE0
aE1
aE2
aE3
aE63





ggg/ZETA/1009 7004.cnv
Tile 3
ver 09/24/01 11:13:39

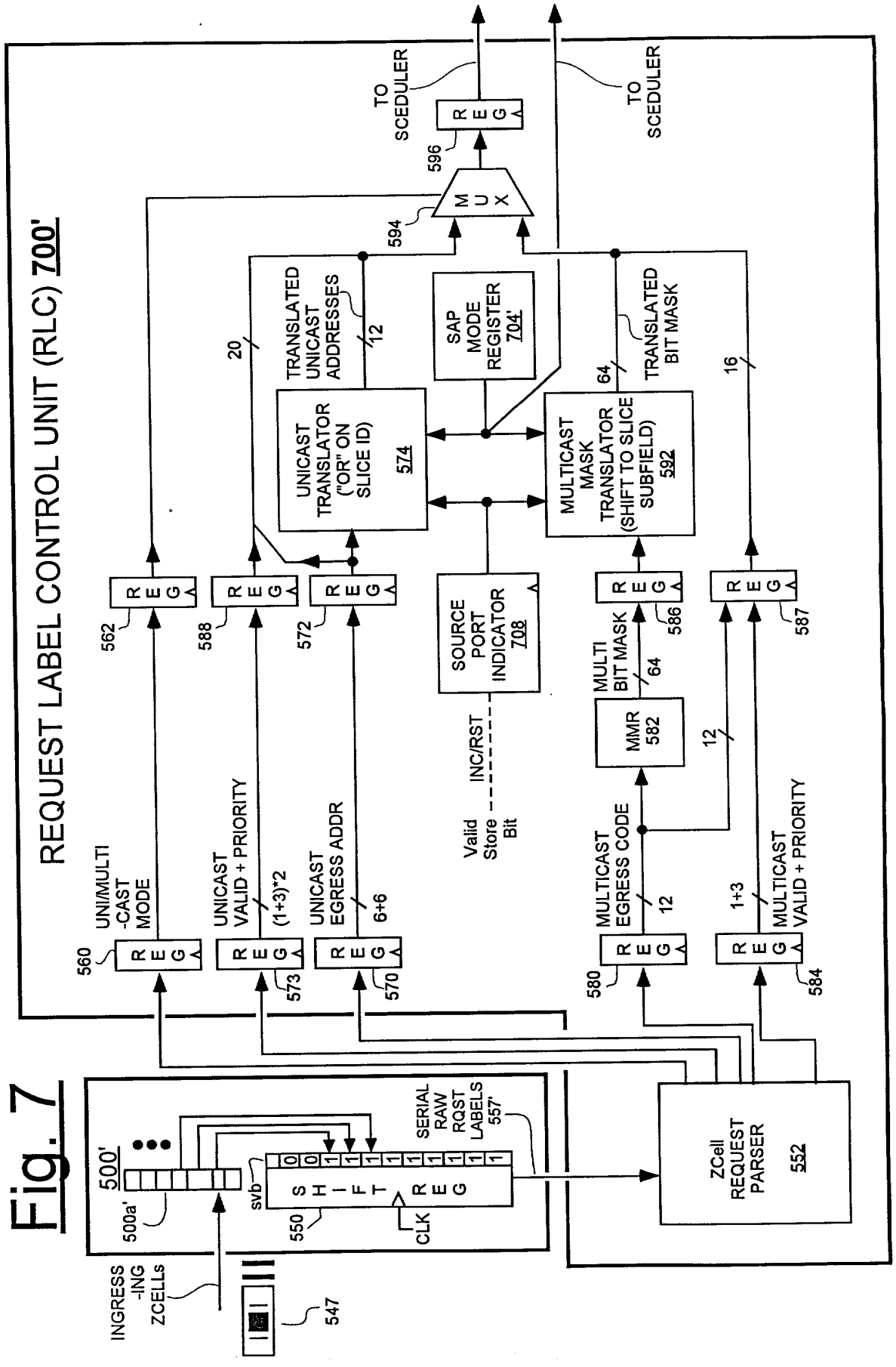


Fig. 7

Sheet 14 /

ggg/ZETA/1009.7004 cnv
Tile 4
ver 10/05/01 18:17.55

Fig. 8A

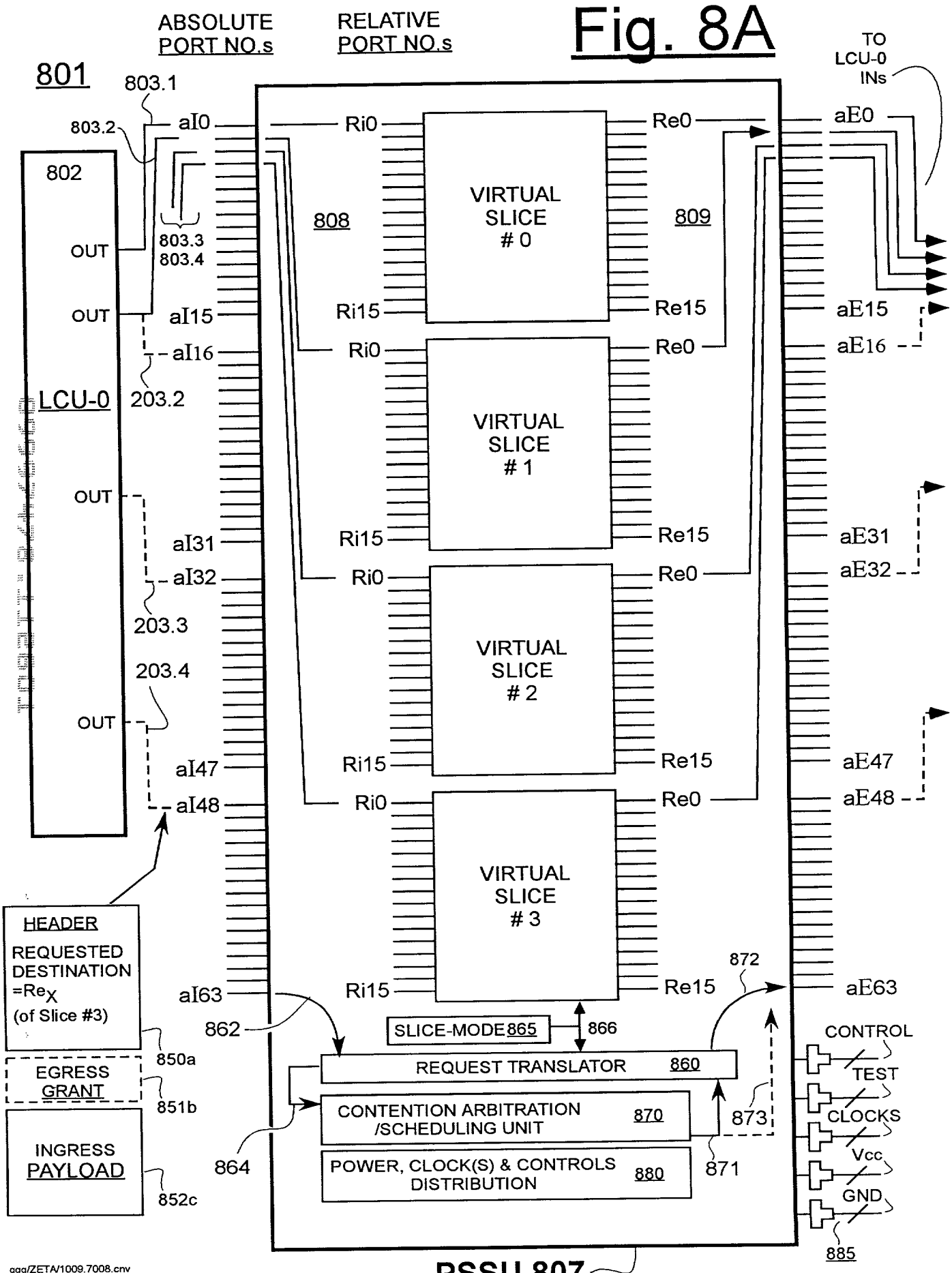

ABSOLUTE PORT NO.s
RELATIVE PORT NO.s
801
803.1
803.2
aI0
802
OUT
803.3
803.4
OUT
aI15
aI16
LCU-0
203.2
OUT
aI31
aI32
203.3
203.4
OUT
aI47
aI48
aI63
HEADER
REQUESTED DESTINATION =ReX (of Slice #3)
850a
EGRESS GRANT
851b
INGRESS PAYLOAD
852c
862
808
Ri0
Ri15
VIRTUAL SLICE # 0
VIRTUAL SLICE # 1
VIRTUAL SLICE # 2
VIRTUAL SLICE # 3
809
Re0
Re15
TO LCU-0 INs
aE0
aE15
aE16
aE31
aE32
aE47
aE48
aE63
872
SLICE-MODE 865
866
REQUEST TRANSLATOR 860
CONTENTION ARBITRATION /SCHEDULING UNIT 870
873
POWER, CLOCK(S) & CONTROLS DISTRIBUTION 880
871
864
CONTROL
TEST
CLOCKS
Vcc
GND
885
PSSU 807

Fig. 8B

807'

SAP-16 MODE (UNCROSSED INPUTS)

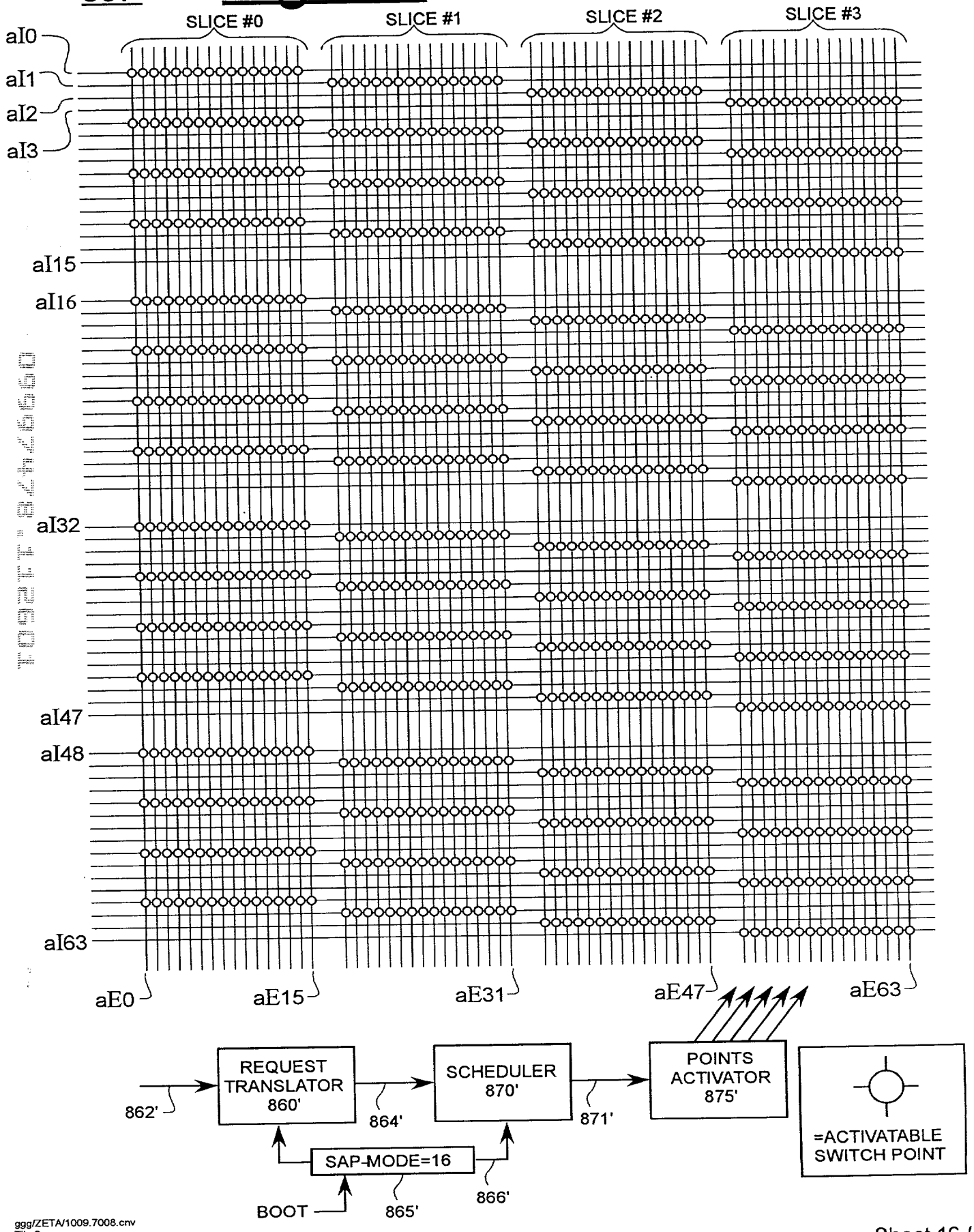


Fig. 8C

SAP-16 MODE (UNCROSSED OUTPUTS & INPUTS)

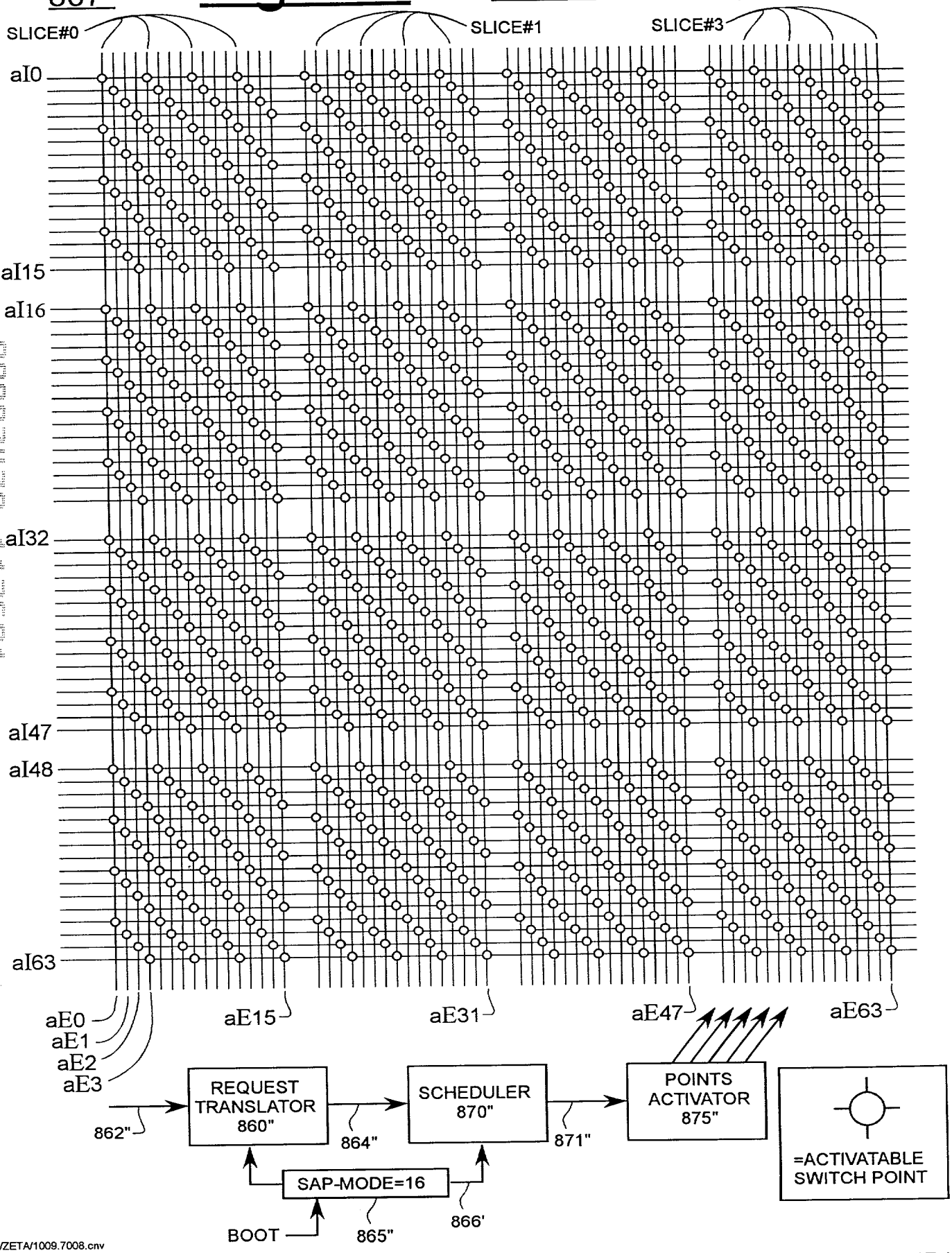


Fig. 8D

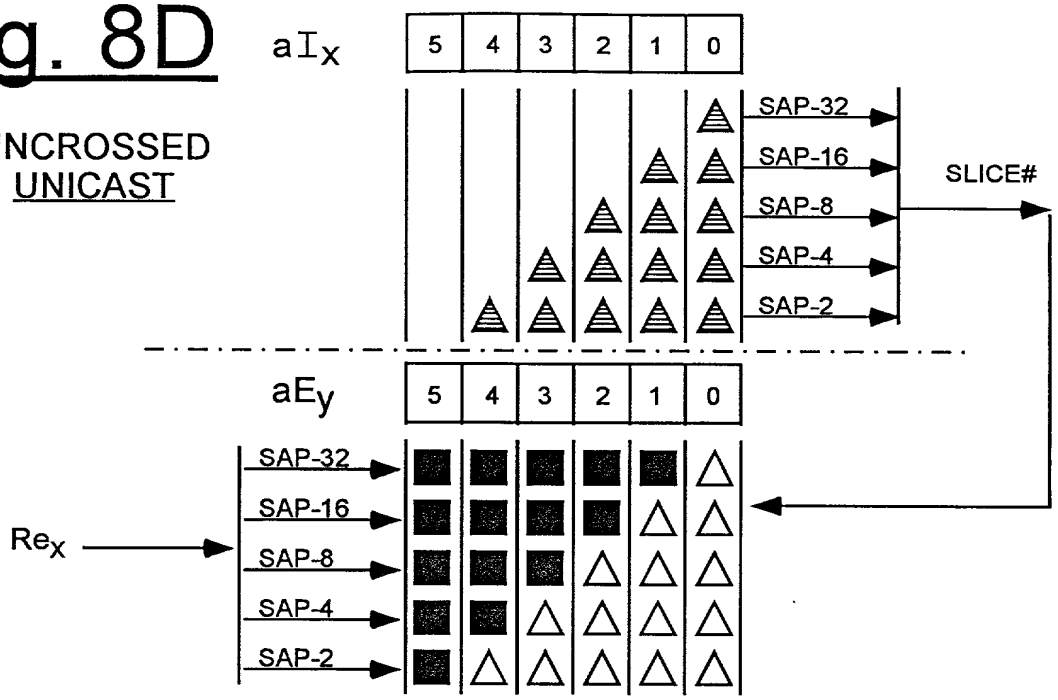

UNCROSSED
UNICAST
aIx
5 4 3 2 1 0
SAP-32
SAP-16
SAP-8
SAP-4
SAP-2
SLICE#
aEy
5 4 3 2 1 0
SAP-32
SAP-16
SAP-8
SAP-4
SAP-2
Rex

Fig. 8E

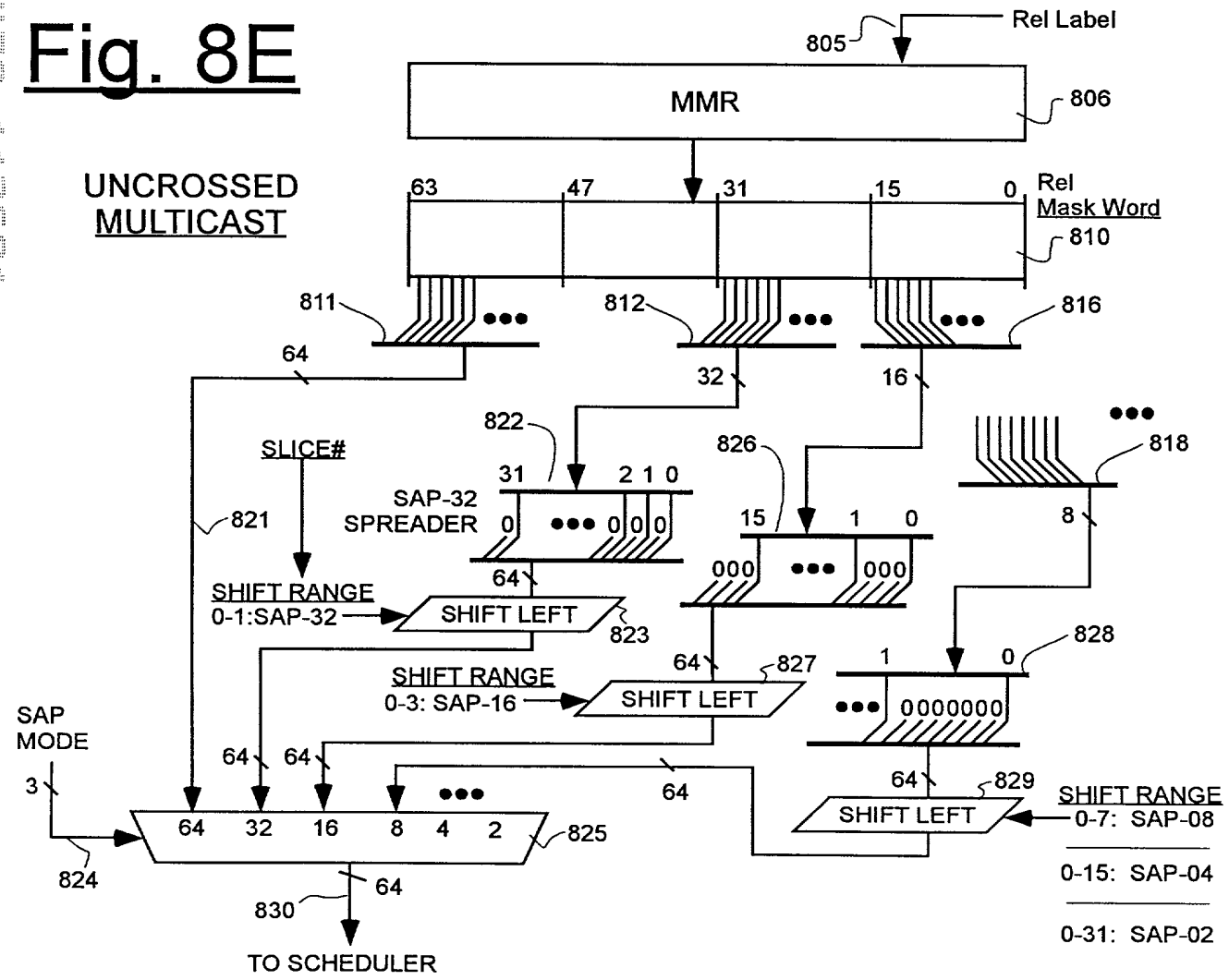

UNCROSSED
MULTICAST
Rel Label
805
MMR
806
63 47 31 15 0
Rel
Mask Word
810
811
812
816
64
32
16
822
826
818
SLICE#
821
31 2 1 0
SAP-32
SPREADER
0 0 0 0
15 1 0
000 000
8
64
SHIFT RANGE
0-1:SAP-32
SHIFT LEFT
823
64
827
1 0
828
SHIFT RANGE
0-3: SAP-16
SHIFT LEFT
0000000
SAP
MODE
3
64 64 64
64
64
829
SHIFT RANGE
0-7: SAP-08
SHIFT LEFT
64 32 16 8 4 2
825
824
0-15: SAP-04
0-31: SAP-02
64
830
TO SCHEDULER

Fig. 8F

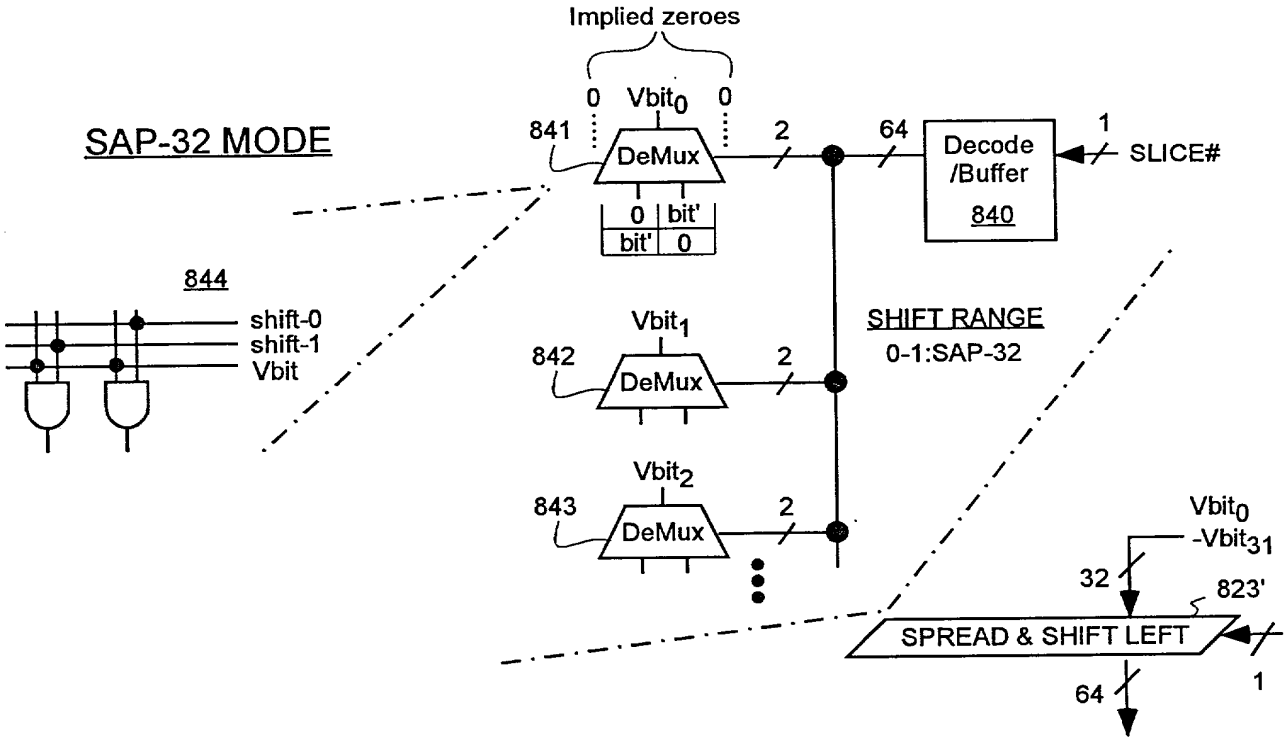
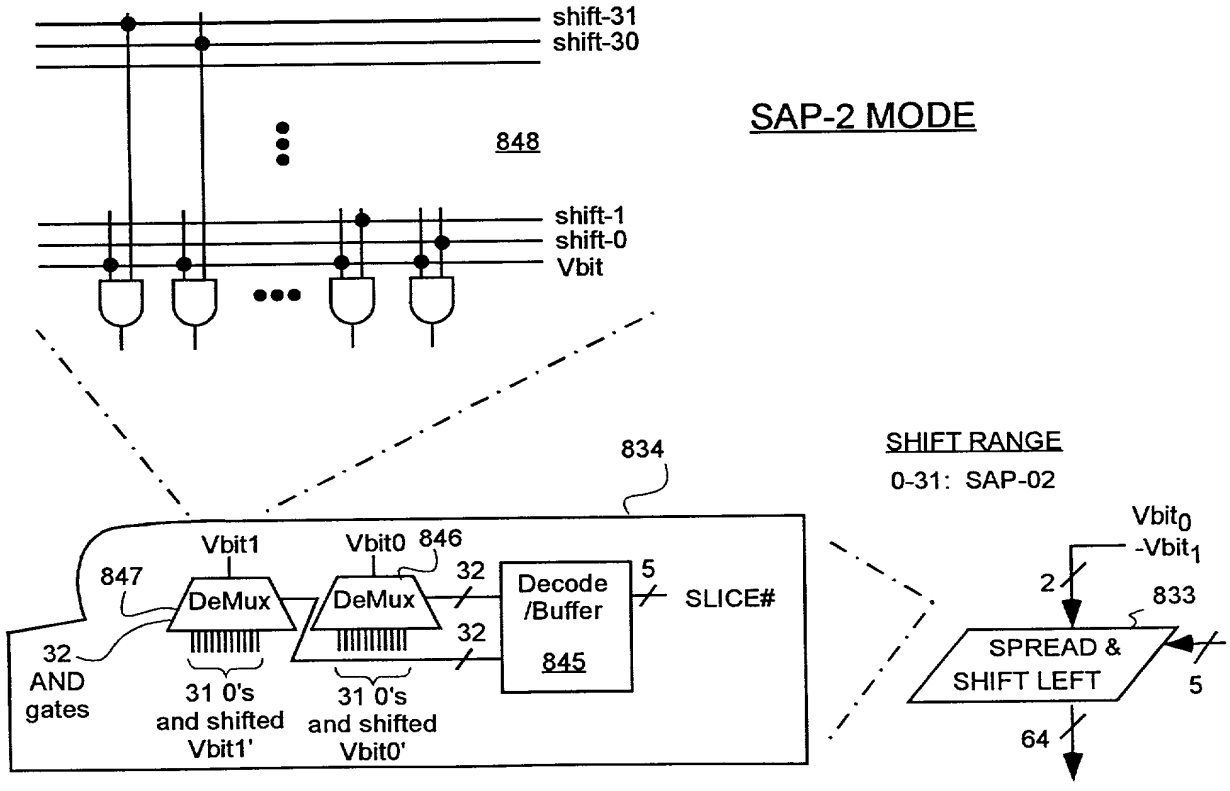

Implied zeroes
SAP-32 MODE
0
Vbit0
0
841
DeMux
2
64
Decode
/Buffer
840
1
SLICE#
0
bit'
bit'
0
844
shift-0
shift-1
Vbit
Vbit1
842
DeMux
2
SHIFT RANGE
0-1:SAP-32
Vbit2
843
DeMux
2
Vbit0
-Vbit31
32
823'
SPREAD & SHIFT LEFT
64
1

Fig. 8G


shift-31
shift-30
848
shift-1
shift-0
Vbit
SAP-2 MODE
834
SHIFT RANGE
0-31: SAP-02
Vbit1
Vbit0
846
847
DeMux
DeMux
32
32
Decode
/Buffer
845
5
SLICE#
32
AND
gates
31 0's
and shifted
Vbit1'
31 0's
and shifted
Vbit0'
Vbit0
-Vbit1
2
833
SPREAD &
SHIFT LEFT
5
64